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Translator's Declaration

I, Yoshinori Tanabe declare that I am thoroughly familiar with both the Japanese and English languages, that the attached document is a true English language translation of Japanese patent application No. 2000-097250 filed in Japan on March 31, 2000 and that all statements made here of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the United States patent application for which this Declaration is filed and any United States patent issuing therefrom.

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Yoshinori Tanabe

Translator's signature

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[Designation of Document] Specification

[Title of the Invention] METHOD OF MANUFACTURING MULTI-LAYERED PRINTED WIRING BOARD

[Claims]

[Claim 1] A method of manufacturing a multi-layered printed wiring board, which is provided with a step of forming an insulating layer made of a photosensitive resin on a substrate for forming a multi-layered printed wiring and subjecting this insulating layer to exposure and development treatment to form a hole having a prescribed shape; a step of coating and forming a curable resin on the insulating layer having a hole formed therein so as to fill the inside of the hole and forming a cured thin film of the curable resin on the surface of the insulating layer by heat treatment; and a step of eliminating the curable resin while leaving the cured thin film, to obtain a via-hole whose aperture width is reduced by the cured thin film.

[Claim 2] The method of manufacturing a multi-layered printed wiring board according to claim 1, wherein the photosensitive resin is made of at least one kind of an epoxy resin, an epoxy-modified acrylate resin, a cationic polymerization product of an epoxy resin, a phenol resin, a melamine resin, a carboxy-modified epoxy acrylate, and a cinnamate.

[Claim 3] The method of manufacturing a multi-layered printed wiring board according to claim 1 or 2, wherein the curable resin is made of a water-soluble resin or a water-soluble cross-linking agent.

[Claim 4] The method of manufacturing a multi-layered printed wiring board according to claim 1 or 2, wherein the curable resin is

made of at least one kind of polymethylsiliceous siloxane, a melamine resin, an acrylate resin, and an epoxy resin.

[Claim 5] A method of manufacturing a multi-layered printing wiring board containing via-holes of plural stages formed by repeating the steps according to claim 1 and constructed such that the upper-stage via-hole has a large degree of reduction than the lower-stage via-hole.

[Claim 6] The method of manufacturing a multi-layered printing wiring board according to claim 3 or 4, wherein the curable resin contains particles of calcium carbonate or polybutadiene rubber.

[Claim 7] The method of manufacturing a multi-layered printing wiring board according to claim 1, wherein the curable resin contains particles of a rubber comprising a butadiene-acrylonitrile copolymer, the method being further provided with a step of chemically roughing the cured thin film.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention Belongs]

The present invention relates to a multi-layered printed wiring board, and particularly to a method of manufacturing a multi-layered printed wiring board formed by successively building up a conductive layer and an insulating layer.

[0002]

[Prior Art]

Following miniaturization and lightening and acceleration and multifunction of electronic instruments, printed wiring boards mounted

with a semiconductor device have rapidly become fine-patterned and multi-layered. In a multi-layered printed wiring board structure by press lamination, it is difficult to form a via capable of realizing continuity between upper and lower circuits in an arbitrary place, and therefore, there has been employed a build-up system of forming a multi-layered printed wiring board by successively laminating an insulating layer and a conductive layer.

[0003]

In multi-layered printed wiring boards by a build-up system, the construction in which an upper layer via and a lower layer via are not piled up each other is general. However, in order to adapt to the acceleration of signals, minimization of circuit patterns is inevitable, and a via-on-via structure in which the upper layer via is piled up and formed on the lower layer via is watched.

[0004]

The process of forming a via is reported in, for example, the following document.

High Density Build-up Technology for Flip Chip Application, Mottoi Asai, p.200, IEMT/IMC Proceedings, 1999

This is one using a photo via process. A process of forming via-on-via of the conventional build-up system will be described below by referring to this.

[0005]

Fig. 6 shows a basic shape of a core substrate 3 from which a multi-layered printed wiring is formed. In the core substrate 3, a wiring pattern

20a comprising lines 40, lands 50, etc., which becomes a first-layer conductive layer, is already formed by photolithography or the like. In the example as illustrated herein, the land (via) pitch is 800 μm, and the land diameter (LD) is 250 μm, and two lines are drawn around with an L/S (line/space) of 100 μm between the lands.

Fig. 7 shows the conventional process of forming via-on-via on the core substrate 3. In this drawing, 1 stands for a first insulating layer made of a photosensitive negative working resist; 11 stands for an insulating layer pattern generated as a result of exposure and development of the first insulating layer 1; 8 stands for a via for ensuring continuity between an upper layer land and a lower layer land; 60 stands for a photomask in which a metal such as Cr is vapor deposited in portions corresponding to the lands 50; an arrow mark designated by 70 stands for ultraviolet ray to be used for the exposure; and 80 stands for a via-hole.

Incidentally, in the case where the members having the same function are formed over a plurality of layers, they are distinguished into ones according to the first layer, second layer, third layer and fourth layer, respectively using suffix letters a, b, c and d accompanying each of the numerals.

[0006]

In Step 1, a first-layer first insulating layer 1a is uniformly spin coated in a thickness of, for example, from about 5 to 70 μm on the core substrate 3. Next, heat treatment (pre-baking) is carried out at from 70 to 150°C to evaporate an excess of a solvent contained in the first insulating layer 1a.

In Step 2, the first insulating layer 1a is exposed to ultraviolet ray through a photomask 60a. In the portion irradiated with ultraviolet ray 70a, reaction components such as acids and radicals are generated, and a cross-linked structure is formed.

In Step 3, development is carried out. When the first insulating layer 1a is rinsed with a developing solution, a portion not irradiated with the ultraviolet ray 70 is dissolved and eliminated. There is thus formed an insulating layer pattern 11a containing via-holes 80a.

[0007]

In Step 4, a conductive resin is embedded in the via-hole to form a via 8a. Further, a second-layer wiring pattern 20b is further formed thereon by, for example, the semi-additive process. The semi-additive process is a process in which after subjecting to entire electroless copper plating, a wiring pattern is formed from a plating resist, and electro-plating is grown only in the wiring portion while making an exposed chemical copper-plated film act as an electrode.

In Step 5, a second-layer first insulating layer 1b is uniformly formed and then pre-baked, if desired in the same manner as in Step 1. In Step 6, ultraviolet ray is exposed through a photomask 60b in the same manner as in Step 2. In Step 7, the second-layer first insulating layer 1b is developed to form a second-layer via-holes 80b in the same manner as in Step 3. In Step 8, a conductive resin is embedded to form a via 8b, followed by successively subjecting to electroless plating treatment and electro-plating treatment to finish a third-layer wiring pattern 20c in the same manner as in Step 4.

According to a series of treatments as described previously, the via-on-via is formed. The size of the resulting via and land is identical in the respective layers, and two lines are formed between the lands.

Incidentally, though photolithography is used herein for forming the via-holes, there is a process of providing an aperture in the insulating layer 1 upon by irradiation of excimer laser or YAG laser without using a photomask.

[0008]

[Problems that the Invention is to Solve]

Now, following high functions of semiconductor devices to be mounted on a multi-layered printed wiring board, the number of input-output pins accompanying the semiconductor device, in its tern the number of lines necessary for wiring patterns greatly increases.

Assuming that the pitch between the via-holes (or lands) is definite, the number of lines capable of being drawn around between the lands can be increased when the size of the via-holes (or lands) is small. Accordingly, it is investigated to make the via-holes small. However, according the conventional process of forming a via-hole, since there is a resolution limit in the photolithography process or restriction in exposure diameter of the laser, it does not satisfactorily proceed to make the via-hole fine. For this reason, it is demanded that the printed wiring board becomes more multi-layered, resulting in problems such as a large increase in manufacturing costs.

[0009]

[Means for Solving the Problems]

The method of manufacturing a multi-layered printed wiring board

according to the invention is provided with a step of subjecting an insulating layer to exposure and development treatment to form a hole having a prescribed shape; a step of coating and forming a curable resin on the insulating layer having a hole formed therein so as to fill the inside of the hole and forming a cured thin film of the curable resin on the surface of the insulating layer by heat treatment; and a step of eliminating the curable resin while leaving the cured thin film, to obtain a via-hole whose aperture width is reduced by the cured thin film.

Also, in the method of manufacturing a multi-layered printed wiring board according to the invention, a material made of at least one kind of an epoxy resin, an epoxy-modified acrylate resin, a cationic polymerization product of an epoxy resin, a phenol resin, a melamine resin, a carboxy-modified epoxy acrylate, and a cinnamate can be used in the photosensitive resin.

Also, in the method of manufacturing a multi-layered printed wiring board according to the invention, a water-soluble resin or a water-soluble cross-linking agent can be used in the curable resin.

Also, in the method of manufacturing a multi-layered printed wiring board according to the invention, a material made of at least one kind of polymethylsiliceous siloxane, a melamine resin, an acrylate resin, and an epoxy resin can be used in the curable resin.

Also, in the method of manufacturing a multi-layered printed wiring board according to the invention, it is possible to make the upper-stage via-hole have a degree of reduction of the aperture width larger than the lower-stage via-hole.

Also, in the method of manufacturing a multi-layered printed wiring board according to the invention, the curable resin can contain particles of calcium carbonate or polybutadiene rubber.

Also, in the method of manufacturing a multi-layered printed wiring board according to the invention, a material containing particles of a rubber comprising a butadiene-acrylonitrile copolymer can be used in the curable resin, and chemically roughing treatment can be carried out.

[0010]

[Mode for Carrying Out the Invention]

Next, the invention will be described below in detail based on the mode illustrated in the drawings. Fig. 1 is a drawing to explain the process of forming a via-hole having a reduced aperture size, which is a basis of the invention.

In Fig. 1, 1 stands for a first insulating layer made of a photosensitive resin, in which when irradiated with light, reaction components such as acids and radicals are generated; 2 stands for a second insulating layer made of a curable resin, in which when heat treated, reaction components such as acids and radicals are generated, and cross-linking reaction occurs; 3 stands for a core substrate in which a wiring pattern 20 comprising lands 50 and lines 40 is formed; 4 stands for a cross-linked layer generated as a result of reaction between the insulating layer 1 and the insulating layer 2 at the interface; and 11 is an insulating layer pattern generated as a result of exposure and development of the first insulating layer 1, in which holes 90 are formed.

[0011]

In Step 1, first of all, a first insulating layer 1 is uniformly formed in a thickness of, for example, from about 5 to 70 μm on a core substrate 3 by a method such as spin coating, curtain coating, dipping, and spray coating. Next, heat treatment (pre-baking) is carried out at from 70 to 150°C for from about 1 to 60 minutes to evaporate an excess of a solvent contained in the first insulating layer 1.

[0012]

In Step 2, the first insulating layer 1 is exposed to ultraviolet ray through a photomask 60. Since this example uses a photosensitive negative working resist in the first insulating layer 1, in the portion irradiated with ultraviolet ray 70, reaction components such as acids and radicals are generated, and a cross-linked structure is formed.

[0013]

In Step 3, the first insulating layer 1 is developed. When the first insulating layer 1 is rinsed with a developing solution, a portion not irradiated with the ultraviolet ray 70 is dissolved and eliminated, whereby holes 90 remain. There is thus formed a insulating layer pattern 11 is formed, but reaction components such as acids and radicals remain at the end portions of an insulating layer pattern 11.

Incidentally, a method in which the first insulating layer 1 is bored upon irradiation with carbon dioxide (CO_2) laser, YAG laser, excimer laser, etc. is also employable in the invention because reaction components such as acids and radicals are generated on the end surfaces of the insulating layer pattern 11.

[0014]

In Step 4, a second insulating layer 2 is uniformly formed in the same manner as in the first insulating layer 1. Next, if desired, this is pre-baked at, for example, 85°C for about 30 minutes.

In Step 5, heat treatment is carried out at a temperature at which the insulating layer pattern 11 does not deform, for example, from about 85 to 160°C. By this heat treatment, the reaction components remaining in the insulating layer pattern 11, such as acids and radicals, diffuse into the second insulating layer 2. When the diffusion of acids, radicals, etc. is promoted, cross-linking reaction starts at the interface between an insulating layer pattern 11a and the second insulating layer 2. In this case, the heat treatment time is, for example, from about 1 to 60 minutes and varies depending on the kind of the insulating layer material to be used and the thickness of the necessary cross-linked layer.

As a result, a cross-linked layer 4 is formed at the interface of the first insulating layer 1 and the second insulating layer 2 so as to cover the insulating layer pattern 11. The cross-linked layer 4 may be said to be a cured resin layer.

[0015]

In Step 6, rinsing is carried out. By rinsing, the uncross-linked portion of the second insulating layer 2 is flown away and eliminated. For rinsing, a solvent that dissolves the uncross-linked portion of the insulating layer 2 but does not dissolve the insulating layer 1 is selected and used among pure water, aqueous solutions mixed with an organic solvent, alkaline developing solutions such as tetramethylammonium hydrate (TMAH) and sodium hydroxide, and organic solvents. As a result, via-holes

80 are formed.

In Step 7, a conductive resin is coated such that a conductor is embedded in the via-hole 80, to form a via 8.

[0016]

The via 8 (and the via-hole 80) formed by the foregoing treatment is reduced in width (diameter) as compared with the size expected from the pattern of a photomask 60.

In this application, since the aperture width of the via-hole is reduced utilizing the cross-linking reaction occurred between the first insulating layer and the second insulating layer, there is neither resolution limit in the photolithography process nor restriction in exposure diameter of the laser. For this reason, the resolution limit of this application largely exceeds that in the conventional measures, and it is possible to open even extremely small-sized via-holes as compared with the conventional ones with good accuracy.

[0017]

It is considered that the reaction components such as acids and radicals contribute to the cross-linking reaction occurred between the first insulating layer and the second insulating layer. Descriptions indicating this are disclosed in the following documents.

(a) Model of acid generation:

Cho-LSI Rejisuto no Bunshi Sekkei (Molecular Design of VLSI Resists), written by Yuzuru Tsuda and published by Kyoritsu Shuppan, p.58 (1990)

(b) Model of radical generation:

Zokanzai (Sensitizers), edited by Katsumi Tokumaru and published by Kodansha, p.154 (1987)

Incidentally, it should not be construed that the invention is limited to the cross-linking reactions caused by acids or radicals. Needless to say, even other reaction components give rise to the same effects so far as reaction components formed by incidence of light and cross-linking reaction or curing reaction caused therefrom are utilized.

[0018]

Next, concrete materials that can be applied to the first insulating layer and the second insulating layer of the invention will be described.

For the first insulating layer, materials that internally generate the reaction components such as acids and radicals by light irradiation or proper heat treatment are employed. If the material is a resist, any of a positive working type and a negative working type may be properly chosen and are not limited by the mode of use such as liquids or films.

Specific examples include epoxy resins, materials containing an epoxy-modified acrylate resin as the major component, cationic polymerization products of an epoxy resin, materials constituted of a phenol resin and a melamine resin, and materials constituted of mixtures thereof. Also, materials constituted of a mixture of a carboxy-modified epoxy acrylate and an epoxy resin and materials constituted of a cinnamate and an epoxy resin are employable.

[0019]

On the other hand, for the second insulating layer 2, materials that when subjected to heat treatment, cause cross-linking reaction in the

presence of reaction components such as acids and radicals and become insoluble in a developing solution are employed. These materials include a wide variety of resins of from water-soluble materials such as water-soluble resins and water-soluble cross-linking agents to water-insoluble, organic solvent-soluble insulating materials and therefore, can be propyl chosen. Also, the second insulating layer is not limited by the mode of use such as liquids or films likewise the first insulating layer.

[0020]

As the water-soluble resins that can be employed in this application, are especially effective polyacrylic acid, polyvinyl acetal, polyvinylpyrrolidone, polyethyleneimine, polyethylene oxide, styrene-maleic acid copolymers, polyvinylamine resins, polyallylamine, and oxazoline group-containing water-soluble resins as illustrated in Fig. 2.

[0021]

Also, water-soluble melamine resins, water-soluble urea resins, water-soluble alkyd resins, and sulfonamide resins can be similarly employed.

Incidentally, these water-soluble resins are not always required to be used singly but can be properly mixed and used.

[0022]

Examples of the water-soluble cross-linking agents that can be employed in this application include urea type cross-linking agents such as urea derivatives, alkoxymethylureas, N-alkoxyethyleneureas, ethyleneurea, and ethyleneureacarboxylic acid; melamine type cross-linking agents such as melamine derivatives and alkoxymethylmelamine derivatives;

benzoguanamine; and glycoluril as illustrated in Fig. 3. These cross-linking agents are properly used singly or in admixture.

Incidentally, though amino type cross-linking agents are enumerated herein, the cross-linking agents are not limited thereto, but any cross-linking agents that when heat treated, cause cross-linking with the reaction components of the first insulating layer can be employed in the invention.

[0023]

Also, the water-soluble resin and the water-soluble cross-linking agent can be mutually mixed and used. Since the water-soluble cross-linking agent includes one that when used alone, cannot form a uniform film, such a cross-linking agent can improve film-forming performance by properly mixing with the water-soluble resin.

Also, a mutual mixture increases storage stability because of its high solubility in water. For example, mixtures of a polyvinyl acetal resin as the water-soluble resin composition with methoxymethylolmelamine or ethyleneurea as the water-soluble cross-linking agent can be stably used even after storing over a long period of time.

[0024]

Examples of the water-insoluble, organic solvent-soluble insulating materials that can be employed in the second insulating layer 2 include polymethylsiliceous siloxane, melamine resins, acrylate resins, and epoxy resins.

In this case, it is important to select a solvent that dissolves the second insulating layer. Solvents that dissolve the second insulating layer

and do not dissolve the first insulating layer but properly swell it are suitable.

Examples include xylene, anisole, tetrahydrofuran, N-methylpyrrolidone, γ-butyrolactone, and MEK (methyl ethyl ketone). These solvents can be used singly or in admixture.

[0025]

Incidentally, the second insulating layer can be mixed with inorganic particles of calcium carbonate, etc. or resin particles of polybutadiene rubber, etc. Also, after forming an insulating layer by mixing with rubber particles comprising a butadiene-acrylonitrile copolymer, the insulating layer may be chemically etched with an oxidizing agent comprising a mixture of potassium hydrogenchromate, sulfuric acid, etc. Thus, the surface of the insulating layer is roughed so that adhesion to the conductor can be enhanced.

[0026]

Next, a method of controlling the cross-linking reaction will be described. The controlling method includes a measure of adjusting the process condition and a measure of adjusting the material formulation of the second insulating layer 2.

In the process controlling measure, (1) a measure of adjusting the heat treatment temperature and treatment time is effective. By adjusting the treatment time while fixing the heating temperature, or adjusting the heating temperature while fixing the heating time, it is possible to accurately control the thickness of the cross-linked layer.

Also, from the standpoint of the material formulation to be used in

the second insulating layer, (2) a measure of mixing two or more kinds of proper water-soluble resins and adjusting a mixing ratio thereof to control the reaction amount with the first insulating layer and (3) a measure of mixing a water-soluble resin with a proper water-soluble cross-linking agent and adjusting a mixing ratio thereof to control the reaction amount with the first insulating layer are effective.

[0027]

The control of such cross-linking reactions is not unitarily determined but is required to be determined while taking into consideration various conditions such as (1) reactivity between the second insulating layer and the first insulating layer, (2) the shape of the first insulating layer pattern and the film thickness, (3) the thickness of the cross-linked layer as required, (4) usable exposure conditions and heat treatment conditions, and (5) coating conditions.

Especially, since the reactivity between the first insulating layer and the second insulating layer is influenced by the formulation of the first insulating layer material, in the case where the invention is actually applied, it is desired to optimize the second insulating layer material while taking into consideration the foregoing factors.

[0028]

Next, the method of manufacturing a multi-layered printed wiring board according to the invention will be described. First of all, in Step 1, a first insulating layer 1a is coated on a core substrate 3. In Step 2, the first insulating layer 1a is irradiated with ultraviolet ray 70a through a photomask 60a. In Step 3, the first insulating layer 1a is developed to form

a first insulating layer pattern 11a comprising via-holes 80a.

In Step 4, the holes are filled with a conductive resin to form a conductive layer inside each via-hole. In addition, a second-layer wiring pattern 20b is further formed thereon by, for example, the semi-additive process.

[0029]

In Step 5, a second-layer first insulating layer 1b is coated. In Step 6, ultraviolet ray 70b is irradiated through a photomask 60b. In Step 7, development is carried out to form holes 90b. The uncross-linked insulating layer is dissolved and eliminated to form a second-layer insulating layer pattern 11b. In Step 8, a second-layer second insulating layer 2b is uniformly coated.

In Step 9, heat treatment is carried out to diffuse the reaction components from the first insulating layer 1b and cause cross-linking reaction in the second insulating layer 2b so as to cover the first insulating layer 1b. According to this treatment, a cross-linked layer 4b that has been insolubilized in a developing solution is formed.

In Step 10, development treatment is carried out, and the uncross-linked portion of the second insulating layer 2b is dissolved and eliminated. According to this operation, via-holes 80b having a reduced aperture width are formed.

[0030]

In Step 11, the via-holes are filled with a conductive resin to form a conductive layer inside each reduced via-hole. In addition, a third-layer wiring pattern 20c is further formed thereon by, for example, the semi-

additive process.

The diameter of the land formed herein can be made smaller than that of the lower layer even when a piling margin of the patterns is identical with that of the second layer because the aperture width of the via-hole directly thereunder is reduced. In this way, since the space between the lands is enlarged, the number of lines to be formed between the lands can be increased. In this example, though two lines are formed between the first layer and the second layer, three lines are formed in the third layer.

[0031]

In Step 12, a third-layer first insulating layer 1c is coated. In Step 13, ultraviolet ray 70c is irradiated through a photomask 60c to expose the first insulating layer 1c. In Step 14, the first insulating layer 1c is developed to form a third-layer first insulating layer pattern 1c comprising holes 90c. In Step 15, a third-layer second insulating layer 2c is coated.

[0032]

In Step 16, heat treatment is carried out to form a third-layer cross-linked layer 4c. Here, the heat treatment is carried out at a higher heat treatment temperature or for a longer heat treatment time as compared with the heat treatment conditions in the case of forming the cross-linked layer 4b in Step 9. In this way, diffusion of the reaction components such as acids and radicals is further promoted so that the film thickness of the cross-linked layer becomes thick. In Step 17, development is carried out, and the uncross-linked second insulating layer 2c is eliminated. As a result, via-holes 80c whose aperture width is further reduced are formed.

[0033]

In Step 18, the via-holes are filled with a conductive resin to form a conductive layer inside each reduced via-hole. In addition, a fourth-layer wiring pattern 20d is further formed thereon by, for example, the semi-additive process.

In the wiring pattern 20d, the space between the lands is further wider than that in the wiring pattern 20c, and therefore, the number of lines to be formed is larger than that in the third layer.

[0034]

In the foregoing description, the case wherein two lines are formed between the lands in each of the first and second layers, three lines are formed in the third layer, and four lines are formed in the fourth layer has been described. However, the number of lines can be properly determined according to the rule of L/S to be used.

[0035]

How this application is effective should be evident from comparison of Fig. 4 with Fig. 7. According to the conventional process, even when the wiring pattern is made multi-layered to three layers, only six lines can be drawn around, whereas according to the embodiment of this application, seven lines can be formed. Assuming that the necessary number of lines is seven, according to the conventional process, a fourth layer must be formed, resulting an increase in costs. Also, when the number of layers is large, reliability of instruments is reduced.

In addition, if it is considered to form four layers of wiring patterns, according to the convention process, eight lines are formed, whereas according to this application, eleven lines can be drawn around. Assuming

that the necessary number of lines is eleven, according to the conventional process, a sixth layer must be formed, and two layers must be made multi-layered in surplus.

In the light of the above, according to this application, since the number of lines that can be drawn around can be increased, the number of layers to be laminated can be decreased, leading to enhancement of reliability of instruments.

[0036]

[Examples]

Example 1:

This is an example of forming the first insulating layer pattern 11. On an FR4 substrate manufactured by Mitsubishi Gas Chemical K.K. (copper foil: 20 μm), lands and lines were formed by etching treatment to obtain the core substrate 3. Subsequently, a photosensitive insulating resin, XP9500CC manufactured Shipley Co. as a cationic polymerization product of an epoxy resin was coated on the core substrate by the curtain coating process and heated and dried at 90°C for 50 minutes. Thus, the first insulating layer 1 having a resin film thickness of 50 μm could be formed.

Next, ultraviolet ray of 3.0 J/cm^2 was irradiated using a UV exposure machine (manufactured by USHIO INC.) in the presence of a photomask having a circular pattern having a diameter of 150 μm, heat treatment (at 90°C for 30 minutes) was further carried out, and development with a 1.3 wt% aqueous solution of sodium hydroxide was then carried out. There was thus obtained the first insulating layer pattern 11 having a via-hole pattern having a diameter of 150 μm.

[0037]

Example 2:

This is an example of preparing the second insulating layer. A polyvinyl acetal resin, Eslec KW3 (100 g) manufactured by Sekisui Chemical Co., Ltd. was successively mixed with methoxymethylolmelamine/cymel 370 (50 g) manufactured by Mitsui Cyanamide K.K., pure water (180 g), and isopropyl alcohol (20 g), and the mixture was stirred at room temperature for 6 hours. The reaction mixture was further mixed with 15 g of each of butadiene-acrylonitrile copolymers having a particle size of 5 μm and 1 μm, respectively, and the mixture was stirred and mixed at room temperature for 6 hours. There was thus obtained a second insulating layer solution.

[0038]

Example 3:

This is an example of examining the relationship between a degree of reduction of via-hole and the heat treatment condition. The second insulating layer solution obtained in Example 2 was coated on the core substrate having formed thereon a via-hole pattern having a diameter of 150 μm as obtained in Example 1 by the curtain coating process and then pre-baked at 80°C for 20 minutes.

Next, the heat treatment was carried out under five conditions of at 120°C for 30 minutes, at 120°C for 45 minutes, at 120°C for 60 minutes, at 130°C for 30 minutes, and at 140°C for 30 minutes, respectively, to diffuse the reaction components from the first insulating layer and proceed with cross-linking reaction. Additionally, spray development with pure water was carried out to eliminate the uncross-linked portion in the second

insulating layer (spray pressure: 2 kg/cm^2).

The diameter of the via-holes formed by these operations is shown in Table 1. In any of the cases, the diameter was smaller than 150 μm, and reliance on heat treatment temperature was found among the resulting hole diameters. That is, when the treatment time was fixed at 30 minutes, the hole diameter became small with an increase of the temperature.

Next, in order to examine the roughing effect, this substrate was dipped and oscillated in a 500 g/L aqueous solution of chromic acid (CrO_3) adjusted at 50°C for 15 minutes. Subsequently, the resulting substrate was dipped in a neutralizing agent, OM950 manufactured by Shipley Co. and then rinsed with water.

Additionally, a copper paste, CPC-8000 manufactured by Sumitomo Bakelite Co. as a conductive resin was embedded in the via-pattern to form a via conductive layer. Thereafter, a Cu layer having a film thickness of 20 μm was formed by the semi-additive process and measured for peel strength (peeling at 90°). The measured value of the peel strength was 950 g/cm so that it was confirmed that a sufficient peel strength could be realized.

[0039]

[Table 1]

Heat treatment condition	Via diameter (μm)
Before heat treatment	150
At 120°C for 30 minutes	130
At 130°C for 30 minutes	100
At 140°C for 30 minutes	70

[0040]

Example 4:

This is another example of examining the relationship between a degree of reduction of via-hole and the heat treatment condition. A photosensitive insulating film material, KS22 manufactured by JSR Corporation as the second insulating layer was coated on the core substrate having formed thereon a via-hole pattern having a diameter of 150 μm as obtained in Example 1 by the curtain coating process and then pre-baked at 90°C for 30 minutes.

Next, the heat treatment was carried out under conditions of at 110°C for 10 minutes, at 110°C for 20 minutes, at 110°C for 30 minutes, and at 135°C for 40 minutes, respectively, to diffuse the reaction components and proceed with cross-linking reaction. Additionally, spray development with pure water was carried out to eliminate the uncross-linked portion (spray pressure: 2 kg/cm^2).

The diameter of the resulting via-holes is shown in Table 2. In any of the cases, the diameter was smaller than 150 μm, and reliance on heat treatment time was found among the resulting hole diameters. That is, when the treatment temperature was fixed at 110°C, the hole diameter became small with an increase of the treatment time.

Next, this substrate was dipped and oscillated in a 500 g/L aqueous solution of chromic acid adjusted at 50°C for 15 minutes. Subsequently, the resulting substrate was dipped in a neutralizing agent, OM950 manufactured by Shipley Co. and then rinsed with water.

Additionally, a copper paste, CPC-8000 manufactured by Sumitomo Bakelite Co. was embedded in the via-pattern to form a via conductive layer. Thereafter, a Cu layer having a film thickness of 20 μm was formed by the

semi-additive process and measured for peel strength (peeling at 90°). The measured value was 950 g/cm so that it was confirmed that a sufficient peel strength could be realized.

[0041]

[Table 2]

Heat treatment condition	Via diameter (μm)
Before heat treatment	150
At 110°C for 10 minutes	120
At 110°C for 20 minutes	100
At 110°C for 30 minutes	80
At 135°C for 40 minutes	40

[0042]

Example 5:

This is a still other example of examining the relationship between a degree of reduction of via-hole and the heat treatment condition. A photosensitive insulating material, Probelec XB7081 manufactured by Ciba Geigy (Vantico) was coated on an FR4 substrate manufactured by Mitsubishi Gas Chemical K.K. and then subjected to exposure, heat treatment and development treatment under the conditions recommended by the manufacturer to form a 150-μm via. Next, a photosensitive interlaminar insulating material, XP9500CC manufactured by Shipley Co. was coated by the curtain coating process and then pre-baked at 90°C for 30 minutes.

Next, the heat treatment was carried out under conditions of at 110°C for 15 minutes, at 120°C for 15 minutes, at 130°C for 15 minutes, and at 135°C for 20 minutes, respectively, to diffuse the radical components from

the insulating layer pattern and proceed with cross-linking reaction at the interface. Additionally, spray development with pure water was carried out to eliminate the uncross-linked portion (spray pressure: 2 kg/cm^2).

The diameter of the resulting via-holes is shown in Table 3 along with the heat treatment condition. In any of the cases, the diameter was smaller than 150 μm, and reliance on heating temperature was found among the resulting hole diameters. That is, when the treatment time was fixed, the hole diameter became small with an increase of the treatment temperature.

Next, this substrate was dipped and oscillated in a 500 g/L aqueous solution of chromic acid adjusted at 50°C for 15 minutes. Subsequently, the resulting substrate was dipped in a neutralizing agent, OM950 manufactured by Shipley Co. and then rinsed with water.

Additionally, a copper paste, CPC-8000 manufactured by Sumitomo Bakelite Co. was embedded in the via-pattern, and thereafter, a Cu layer having a film thickness of 20 μm was formed by the semi-additive process and measured for peel strength (peeling at 90°). The measured value was 950 g/cm so that it was confirmed that a sufficient peel strength could be realized.

[0043]

[Table 3]

Heat treatment condition	Via diameter (μm)
Before heat treatment	150
At 110°C for 15 minutes	120
At 120°C for 15 minutes	100
At 130°C for 15 minutes	80
At 135°C for 20 minutes	45

[0044]

Example 6:

This is an example of forming a build-up system multi-layered printed wiring comprising four layers of wiring patterns using the materials and processes shown in Example 4. However, a 1% NaOH aqueous solution was used in place of the pure water spraying in the development of the second insulating layer.

The process flow is shown in Fig. 5. This flow is basically identical with that shown in Fig. 4, and therefore, only the essential points will be described below.

As the core substrate, was used one in which the via pitch is 800 μm, and four lines with an L/S of 50 μm were formed between the lands.

In Step 4, assuming that a piling margin of patterns is 100 μm against the via-hole having a diameter of 150 μm, the land diameter was set up at 250 μm. Since the space between the lands was 550 μm, four lines with an L/S of 50 μm were formed between the lands.

The second-layer second insulating layer 2b was heat treated at 110°C for 20 minutes. When development was carried out, the aperture size of the via-hole was reduced to 100 μm. Assuming that a piling margin is equal to 100 μm as in the second-layer wiring pattern, the third-layer land diameter was set up at 200 μm. Since the via-hole was reduced, and the space between lands was enlarged to 600 μm, five lines with an L/S of 50 μm could be formed between the lands.

The third-layer second insulating layer 2c was heat treated at 135°C

for 40 minutes. When development treatment was carried out, the via-hole was reduced to 40 μm. Following this, assuming that a piling margin is 100 μm, the third-layer land diameter was set up at 140 μm. Since the space between lands was enlarged to 660 μm, six lines with an L/S of 50 μm could be formed between the lands.

[0045]

[Advantage of the Invention]

According to the method of manufacturing a multi-layered printed wiring board of the invention, since it is provided with a step of subjecting an insulating layer to exposure and development treatment to form a hole having a prescribed shape; a step of coating and forming a curable resin on the insulating layer having a hole formed therein so as to fill the inside of the hole and forming a cured thin film of the curable resin on the surface of the insulating layer by heat treatment; and a step of eliminating the curable resin while leaving the cured thin film, to obtain a via-hole whose aperture width is reduced by the cured thin film, it is possible to control the aperture width of the via-hole with good accuracy.

Also, according to the method of manufacturing a multi-layered printed wiring board of the invention, materials such as an epoxy resin, an epoxy-modified acrylate resin, a cationic polymerization product of an epoxy resin, a phenol resin, a melamine resin, a carboxy-modified epoxy acrylate, and a cinnamate can be used in the photosensitive resin.

Also, according to the method of manufacturing a multi-layered printed wiring board of the invention, water-soluble materials such as water-soluble resins and water-soluble cross-linking agents can be used in

the curable resin.

Also, according to the method of manufacturing a multi-layered printed wiring board of the invention, organic solvent-soluble materials such as polymethylsiliceous siloxane, a melamine resin, an acrylate resin, and an epoxy resin can be used in the curable resin.

Also, according to the method of manufacturing a multi-layered printed wiring board of the invention, since the upper-stage via-hole is larger in a degree of reduction of the aperture width than the lower-stage via-hole, it is possible to increase the number of lines that can be drawn around between the lands in the upper stage.

Also, according to the method of manufacturing a multi-layered printed wiring board of the invention, since the curable resin contains particles of calcium carbonate or polybutadiene rubber, it is possible to enhance an adhesive strength of the conductor pattern.

Also, according to the method of manufacturing a multi-layered printed wiring board of the invention, since the curable resin contains particles of a rubber comprising a butadiene-acrylonitrile copolymer, it is possible to enhance an adhesive strength of the conductor pattern by chemical treatment.

[Brief Description of the Drawings]

[Fig. 1]

A process flow diagram to explain the process of forming a via-hole having a reduced aperture width according to the invention.

[Fig. 2]

A drawing to show molecular structures of water-soluble resins to be

used in a second insulating layer according to the invention.

[Fig. 3]

A drawing to show molecular structures of water-soluble cross-linking agents to be used in a second insulating layer according to the invention.

[Fig. 4]

A process flow diagram to explain the process of forming via-on-via according to the invention.

[Fig. 5]

A process flow diagram to explain the process of forming a multi-layered printed wiring board used in Example 6.

[Fig. 6]

A drawing to show the basic shape of a core substrate.

[Fig. 7]

A process flow diagram to explain the conventional process of forming via-on-via.

[Description of Reference Numerals and Signs]

1: First insulating layer

2: Second insulating layer

3: Core substrate

4: Cross-linked layer

8: Via

11: First insulating layer pattern

20: Wiring pattern

40: Line

50: Land

60: Photomask

70: Ultraviolet ray

80: Via-hole

90: Hole

[Designation of Document] Drawings

FIG.1

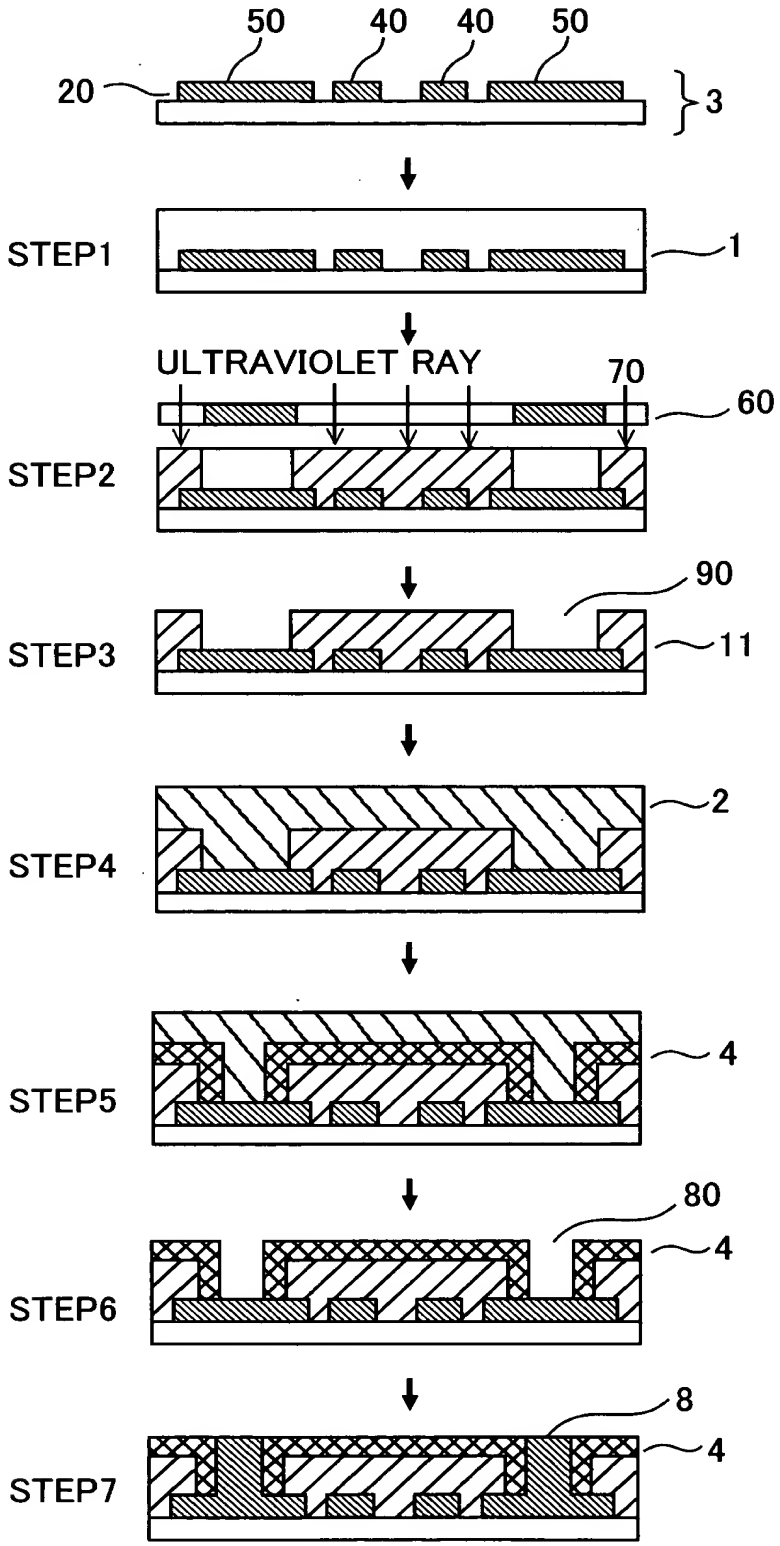
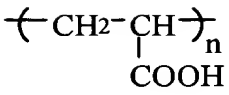
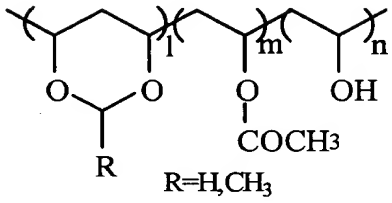


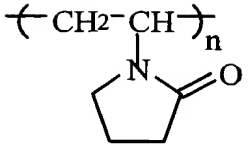
FIG.2



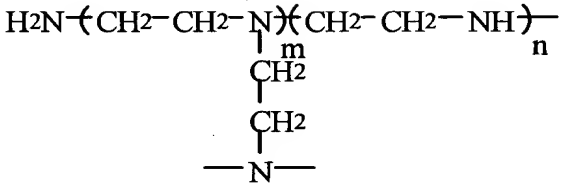
polyacrylic acid



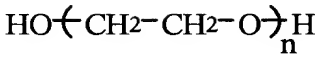
polyvinyl acetal



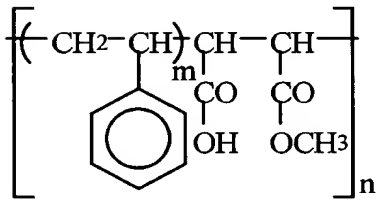
polyvinyl pyrrolidone



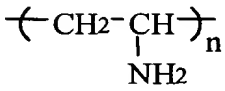
polyethyleneimine



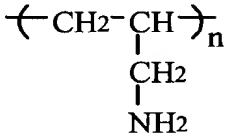
polyethylene oxide



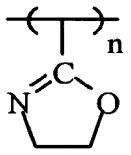
styrene–maleic acid copolymer



polyvinylamine resin

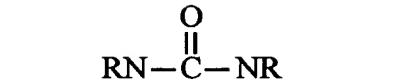


polyallylamine



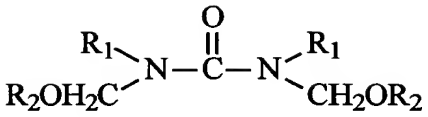
oxazoline group–containing
water–soluble resin

FIG.3



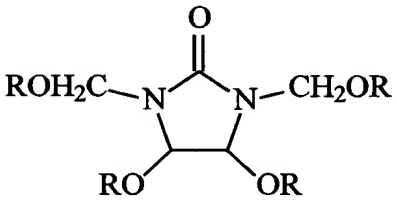
R=H,CH3,CH2OMe,CH2OEt

ureaderivatives



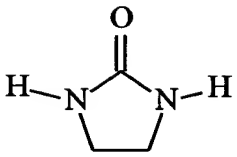
R1=H,CH3,CH2OMe,CH2OEt
R2=H,CH3,Et

alkoxymethylurea

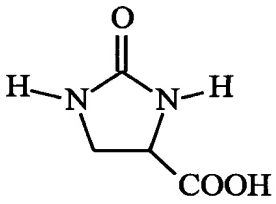


R=H,CH3,Et

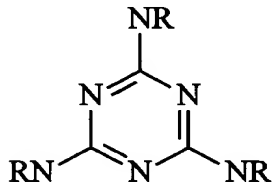
N-alkoxyethyleneurea



ethyleneurea

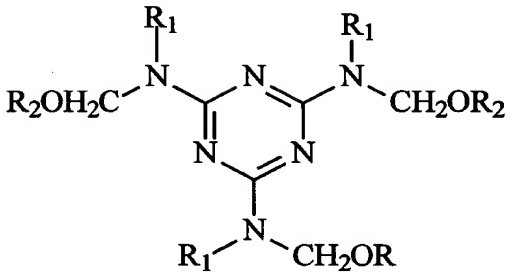


ethyleneureacarboxylic acid



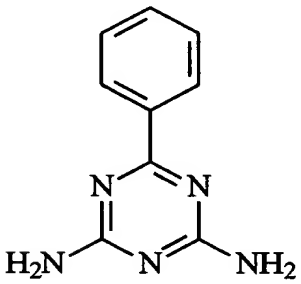
R=H,CH3,CH2OMe,CH2OEt

melamine derivatives

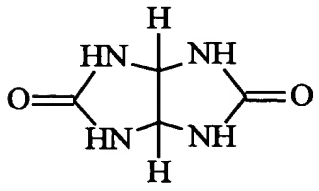


R1=H,CH3,CH2OMe,CHOEt
R2=H,CH3

alkoxymethylmelamine derivatives



benzoguanamine



glycoluril

FIG.4

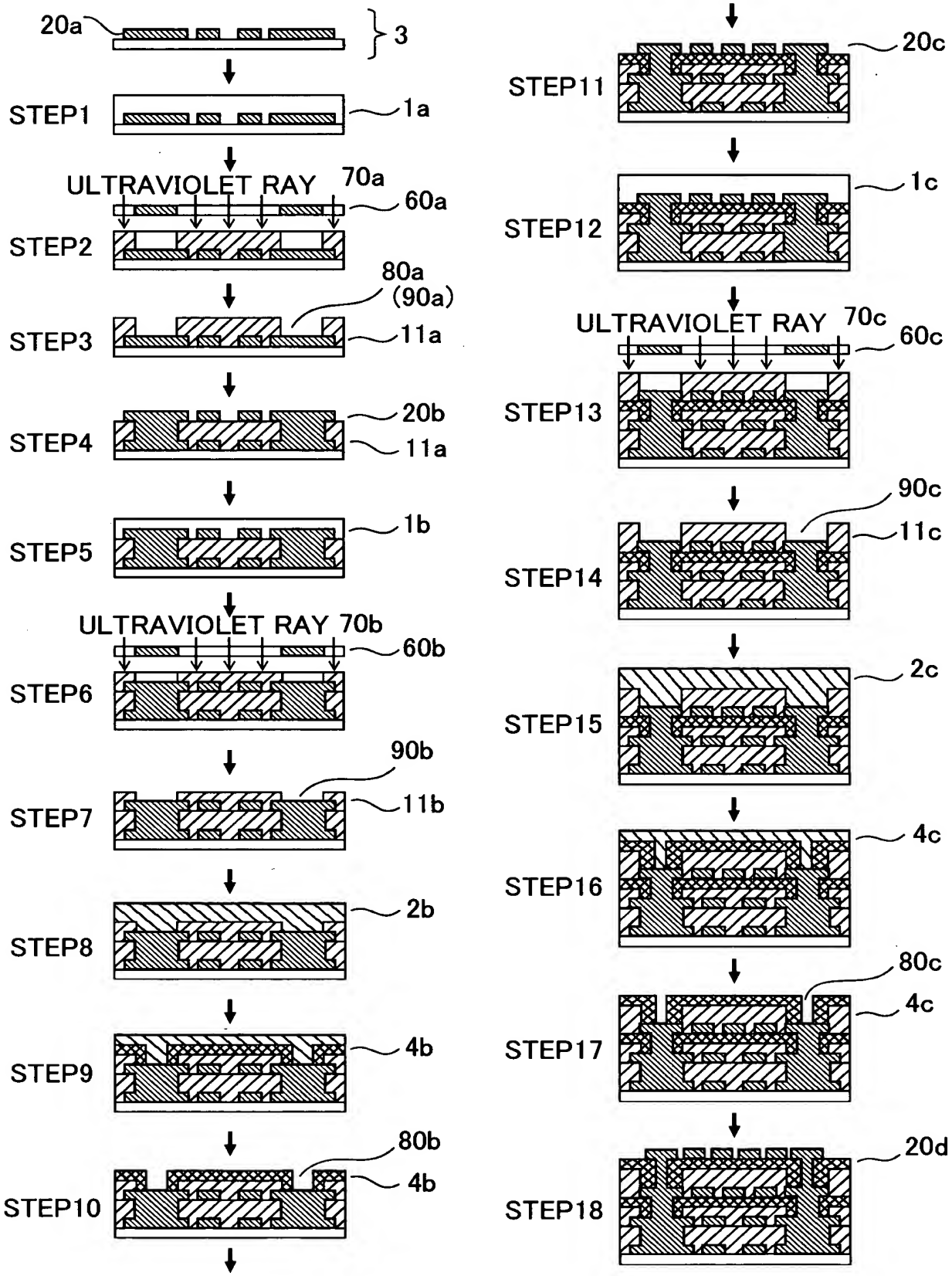

20a
3
STEP1
1a
ULTRAVIOLET RAY
70a
60a
STEP2
80a
(90a)
STEP3
11a
20b
STEP4
11a
STEP5
1b
ULTRAVIOLET RAY
70b
60b
STEP6
90b
STEP7
11b
STEP8
2b
STEP9
4b
80b
STEP10
4b
STEP11
20c
STEP12
1c
ULTRAVIOLET RAY
70c
60c
STEP13
90c
STEP14
11c
STEP15
2c
STEP16
4c
80c
STEP17
4c
STEP18
20d

FIG.5

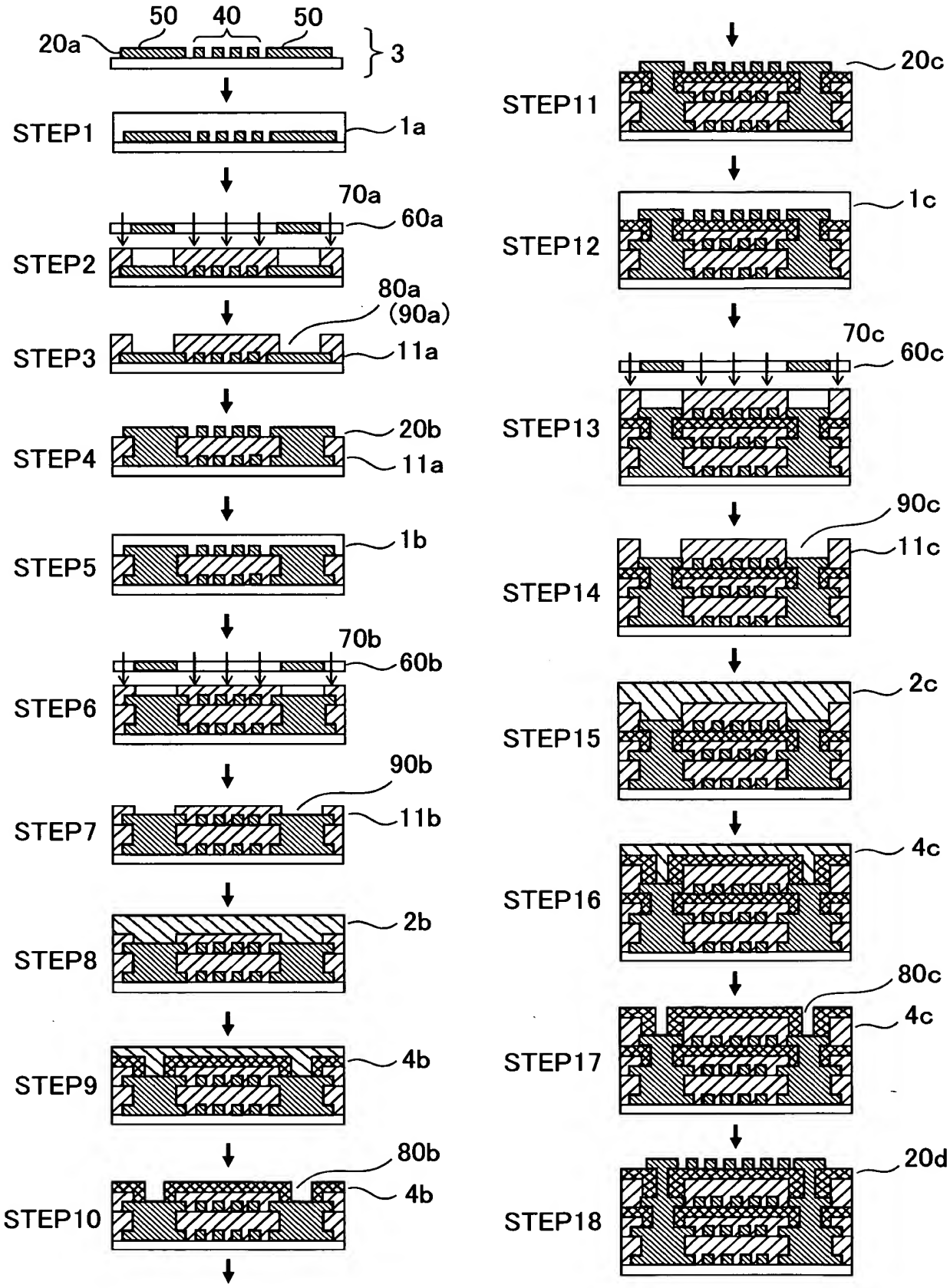

50
40
50
20a
3
STEP1
1a
70a
60a
STEP2
80a
(90a)
STEP3
11a
20b
STEP4
11a
STEP5
1b
70b
60b
STEP6
90b
STEP7
11b
STEP8
2b
STEP9
4b
80b
STEP10
4b
STEP11
20c
STEP12
1c
70c
60c
STEP13
90c
STEP14
11c
STEP15
2c
STEP16
4c
80c
STEP17
4c
STEP18
20d

FIG.6

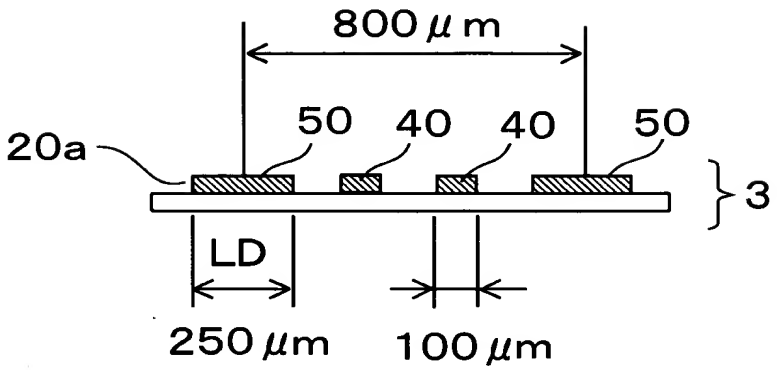
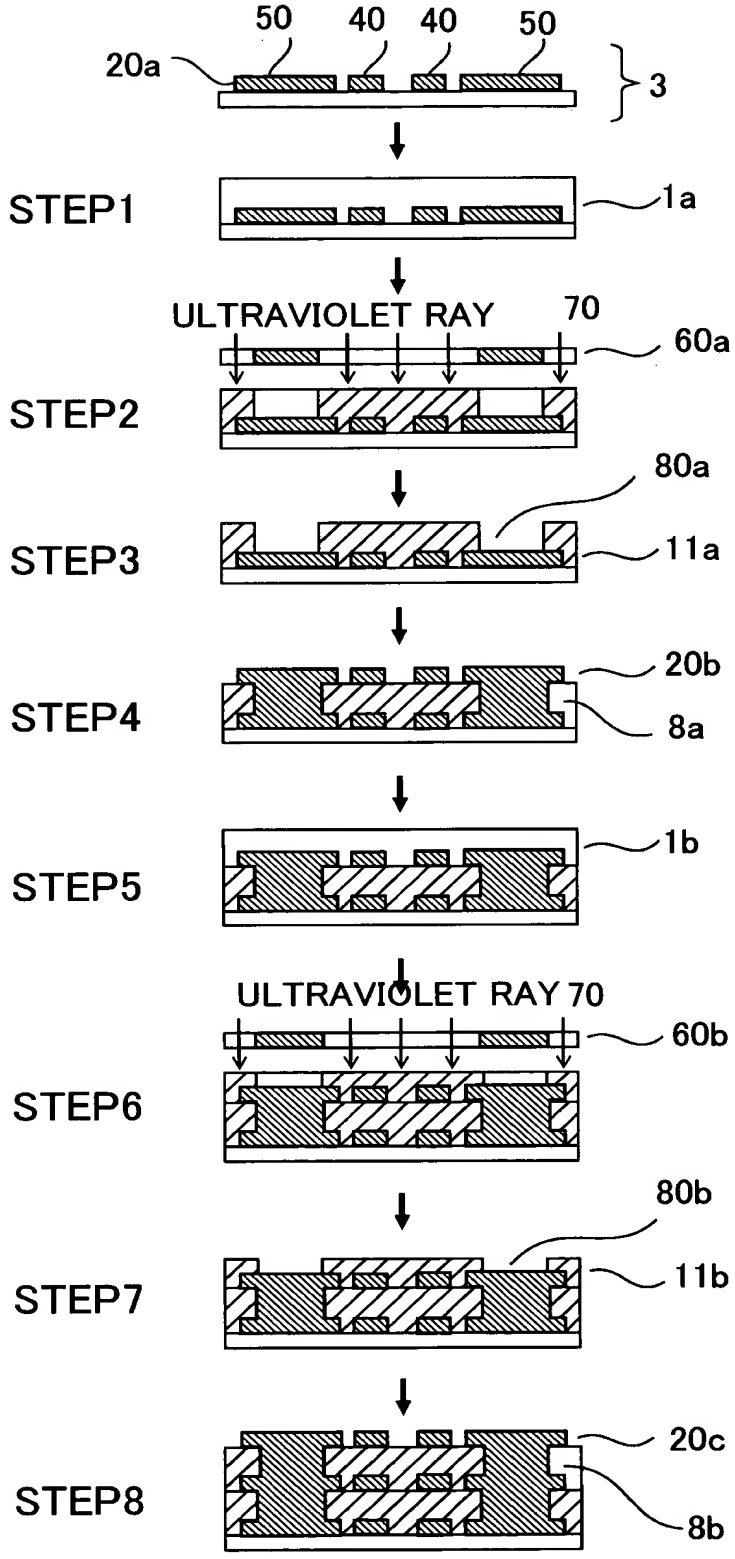


FIG.7


50
40
40
50
20a
3
STEP1
1a
ULTRAVIOLET RAY
70
60a
STEP2
80a
STEP3
11a
20b
STEP4
8a
1b
STEP5
ULTRAVIOLET RAY 70
60b
STEP6
80b
STEP7
11b
20c
STEP8
8b

[Designation of Document] Abstract

[Abstract]

[Problem] In the conventional process of forming a via-hole, since there is a resolution limit in the photolithography process or restriction in exposure diameter of the laser, it was difficult to form a fine via-hole. For this reason, in multi-layered printed wiring boards, the number of lines that can be drawn around between lands was restricted.

[Means for Resolution] A multi-layered printed wiring board is manufactured through a step of forming an insulating layer made of a photosensitive resin on a substrate for forming a multi-layered printed wiring and subjecting this insulating layer to exposure and development treatment to form a hole having a prescribed shape; a step of coating and forming a curable resin on the insulating layer having a hole formed therein so as to fill the inside of the hole and forming a cured thin film of the curable resin on the surface of the insulating layer by heat treatment; and a step of eliminating the curable resin while leaving the cured thin film, to obtain a via-hole whose aperture width is reduced by the cured thin film.

[Selected Drawing] Fig. 1